NORTH SOUTH UNIVERSITY

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

CSE425Concepts of Programming Languages.

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Submitted By :

- Thamid Hasan Pranto - 1711697042
- Md. Haidaruzzaman - 1610977042

Faculty : Md. Shahriar Karim (MSK1)

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Why should we learn Programming Languages?

1. To increase the capability to express and gain more control over the programming language.
2. Knowing the language makes strong background for one to choose the appropriate language.
3. To use the language more effectively.
4. To know the fascinating way of a programming that one have never thought before.
5. To learn new language more easily.
6. To have a better understanding of the significance of implementation.
7. Overall advancement of computing.

Von Neumann Architecture :

Reprogramming instructions are heavily seen computer architecture. No one is going to buy a new hardware system to execute some specific instruction. Rather they would like to see the existing system executing different types of instructions and the same system performing multiple tasks. Von Neumann architecture fulfills this basic need.

Von Neumann architecture was first published by John Von Neumann in 1945.

This computer architecture design consists of a Control Unit, Arithmetic and Logic Unit (ALU), Memory Unit, Registers and Inputs/Outputs.

The main concept of this architecture is to separate the memory form the CPU. The memory contains data and instructions at the same time meaning that, data can be both raw data or instruction. This design is still used in most computers produced today.

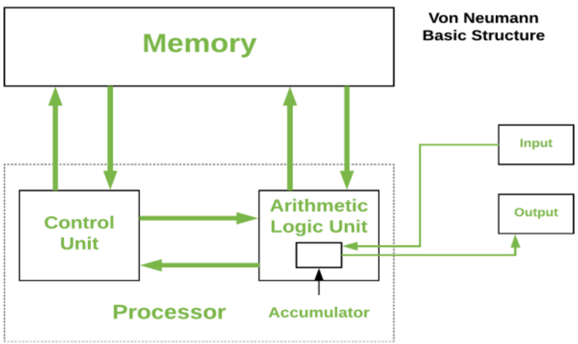


Figure: Von Neumann Architecture

Central Processing Unit (CPU):

The Central Processing Unit (CPU) is the electronic circuit responsible for executing the instructions of a computer program.It is also called as processor.

The CPU consists of Control Unit, Arithmetic Logic Unit and registers.

1.Control Unit: Governs the flow of information through the system and also determines the order of execution of the instructions. The control unit also provides the timing and control signals required by other computer components.

2.Arithmetic Logic Unit: The ALU allows arithmetic (add, subtract etc) and logic (AND, OR, NOT etc) operations to be carried out.

3.Register: Registers are small memory storage to store and transfer data and instruction. Registers are very fast memory storage.

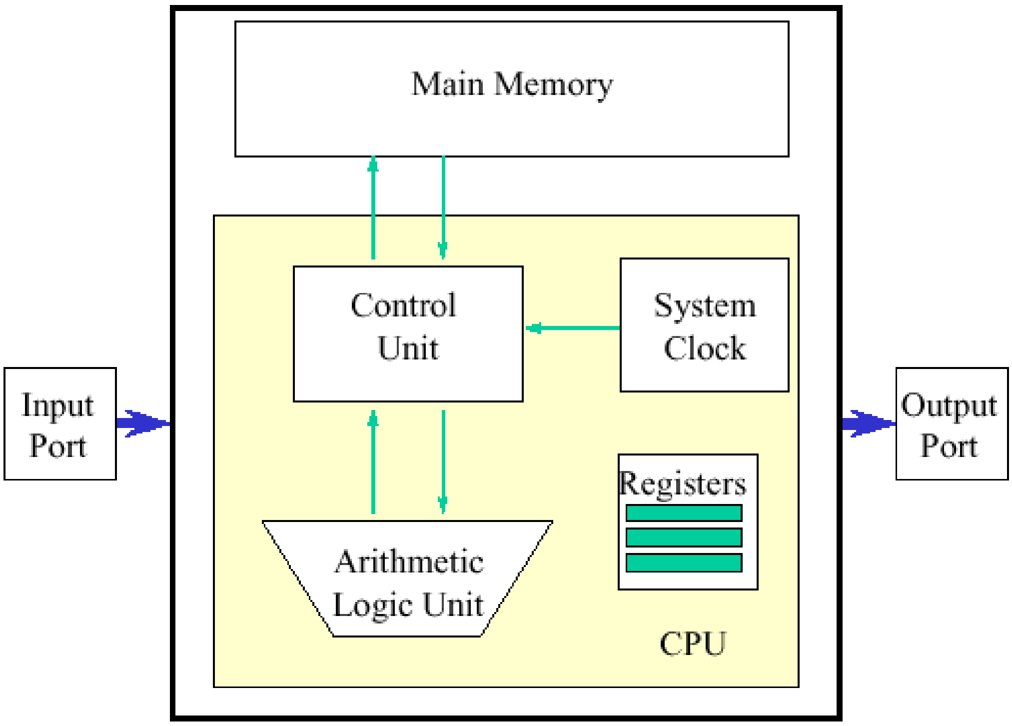


Figure: Central Processing Unit

Memory:

Computer memory is any physical device capable of storing information temporarily, like RAM (random access memory), or permanently, like ROM (read-only memory).Memory unit in Von Neumann is separated into two sections. RAM & ROM

RAM (Random Access Memory): Every data manipulation are first bought into ram and after that the execution process begins. Data comes in the ram for shorter period of time. Ram gets erased during system shutdown. Ram is also referred to as the primary memory. Loading data from permanent memory (hard drive), into the faster and directly accessible temporary memory (RAM), allows the CPU to operate much quickly.

ROM (Read Only Memory): Rom is the permanent data storage of the system. There are certain data which we want to store for a longer period of time. We use ROM for this purpose. ROM data never gets deleted unless deleted on purpose or hardware crash.

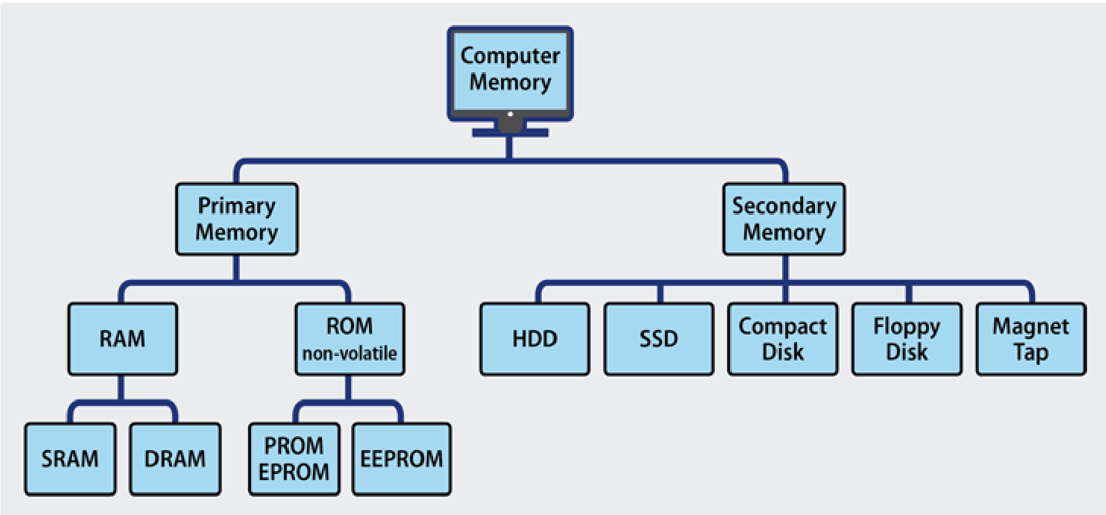


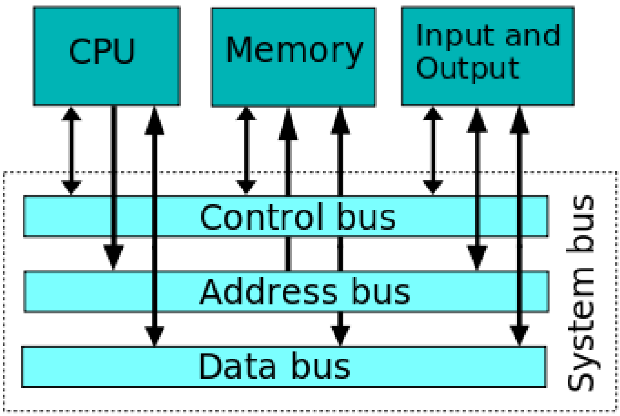
Figure: Computer Memory

BUS:

Buses are the connecting lines by which information is shared between the registers in a multiple-register configuration system.

A bus structure consists of a set of common lines, one for each bit of a register, through which binary information is transferred one at a time. Control signals determine which register is selected by the bus during each particular register transfer.

Von Neumann Architecture comprised of three major bus systems for data transfer.



Address Bus : Address Bus carries the address of data (but not the data) between the processor and the memory.

Data Bus: Data Bus carries data between the processor, the memory unit and the input/output devices.Data bus is bidirectional.

Control Bus: Control Bus carries signals/commands from the CPU

Bottleneck of Von Neumann Architecture :

The Von Neumann bottleneck was described by John Backus in his 1977 ACM Turing Award lecture.
The shared bus between the program memory and data memory leads to the von Neumann bottleneck, the limited throughput (data transfer rate) between the central processing unit (CPU) and memory compared to the amount of memory. Because the single bus can only access one of the two classes of memory at a time, throughput is lower than the rate at which the CPU can work. This seriously limits the effective processing speed when the CPU is required to perform minimal processing on large amounts of data. The CPU is continually forced to wait for needed data to move to or from memory. Since CPU speed and memory size have increased much faster than the throughput between them, the bottleneck has become more of a problem, a problem whose severity increases with every new generation of CPU.

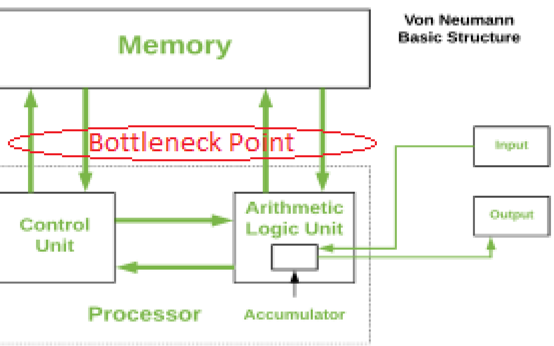


Figure: Von Neumann Architecture bottleneck.

Influence of Von Newman Architecture in Language Design:

The basic architecture of computers has had a profound effect on language design. When we deploy/run a program, it resides in a memory and gets executed by the CPU. Therefore, instructions and data must be transmitted, or piped, from memory to the CPU.Results of operations in the CPU must be moved back to memory. For various operations, there are registers like program counter, instruction register etc. Each instruction execution inside the CPU is determined and controlled by the program counter. And program counter gets its nessasery information from instruction register. This whole idea of Von neumanns architecture, created some ideas that must be present in a language.

- Concept of variable - to model the memory cells, for the assignment statements which are based on the piping operation, we need variables.

- Iterative form of Repetition - Instead of doing a task separately as many times as it is needed, Von Neumann Architecture encourages iterative form of repetition as the instructions are stored in adjacent cells of memory and repeating the execution of a section of code requires only a branch instruction.

Fetch and Execute Cycle:

The sequence of actions that a central processing unit performs to execute each instruction in a program is called the fetch execution cycle.The fetch- execute cycle can be simply described by the following algorithm:

- At the beginning of each cycle the CPU presents the value of the program counter on the address bus. The CPU then fetches the instruction from main memory (possibly via a cache and/or a pipeline) via the data bus into the instruction register.

- From the instruction register, the data forming the instruction is decoded and passed to the control unit which sends a sequence of control signals to the relevant function units of the CPU to perform the actions required by the instruction such as reading values from registers, passing them to the ALU to add them together and writing the result back to a register.
  The “decode the instruction” step in the algorithm means the instruction is examined to determine what action it specifies.

- The program counter is then incremented to address the next instruction and the cycle is repeated.The fetch and execute cycle can easily be described by the algorithm:

```
Initialize the program counter
repeat forever
        fetch the instruction printed to by the program counter
        increment the program counter to point to the next instruction.
        decode the instruction
        execute the instruction
end repeat
```

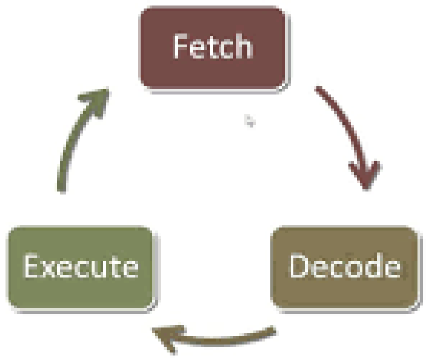


Figure: Fetch and Execute cycle.